CLAIMS

We claim:

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1. A metal-insulator-semiconductor device, comprising:

a semiconductor substrate including a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall; and

a drain region of said first conductivity type adjacent to said body region and to said sidewall,

wherein a stress in said substrate along a bottom portion of said trench does not change appreciably and wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second insulative layer along said bottom portion of said trench, said second insulative layer being coupled to said first insulative layer and said second insulative layer being thicker than said first insulative layer.

2. The MIS device of Claim 1, further comprising a gate region coupled to said first insulative layer and said second insulative layer within said trench.

3. The MIS device of Claim 2, wherein said gate region comprises polysilicon.

4. The MIS device of Claim 1, further including a high conductivity region of said first conductivity type formed in said drain region adjacent to at least said bottom portion of said trench.

5. The MIS device of Claim 1, wherein said first insulative layer comprises an oxide.

6. The MIS device of Claim 1, wherein said second insulative layer comprises an oxide.

7. The MIS device of Claim 1, wherein said second insulative layer comprises a multi-layer insulative layer.

8. The MIS device of Claim 1, wherein said MIS device comprises a MOSFET.

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9. A trench-gate MOSFET, comprising:

a semiconductor substrate including a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall,

wherein a stress in said substrate along a bottom portion of said trench does not change appreciably and wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second insulative layer along said bottom portion of said trench, said second insulative layer being coupled to said first insulative layer and said second insulative layer being thicker than said first insulative layer; and

a gate region coupled to said first insulative layer and said second insulative layer within said trench.

10. The trench-gate MOSFET of Claim 9, wherein said gate region comprises polysilicon.

11. The trench-gate MOSFET of Claim 9, further including a high conductivity region of said first conductivity type formed in said drain region adjacent to at least said bottom portion of said trench.

12. The trench-gate MOSFET of Claim 9, wherein said first insulative layer comprises an oxide.

13. The trench-gate MOSFET of Claim 9, wherein said second insulative layer comprises an oxide.

14. The trench-gate MOSFET of Claim 9, wherein said second insulative layer comprises a multi-layer insulative layer.

15. A trench-gate MOSFET, comprising:

a semiconductor substrate including a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

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a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being coupled to said first insulative layer,

wherein a thickness of a transition insulative layer at the juncture of said first insulative layer and said second insulative layer is not less than a thickness of said first insulative layer; and

a gate region coupled to said first insulative layer and said second insulative layer within said trench.

16. The trench-gate MOSFET of Claim 15, further including a high conductivity region of said first conductivity type formed in said drain region adjacent to at least said bottom portion of said trench.

17. A trench-gate MOSFET, comprising:

a semiconductor substrate including a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

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a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being coupled to said first insulative layer,

wherein a first diameter of said trench taken at a vertical midpoint of said second insulative layer is not greater than a second diameter of said trench taken adjacent to said body region; and

a gate region coupled to said first insulative layer and said second insulative layer within said trench.

18. The trench-gate MOSFET of Claim 17, further including a high conductivity region of said first conductivity type formed in said drain region adjacent to at least said bottom portion of said trench.

19. A method of fabricating an MIS device, comprising:

providing a semiconductor substrate;

forming a trench in said substrate, said trench including a sidewall and a bottom;

depositing a thick insulative layer on said sidewall and said bottom;

depositing a mask layer in said trench;

etching said mask layer to expose a portion of said thick insulative layer on said sidewall while leaving a portion of said mask layer at said bottom of said trench;

etching said thick insulative layer to form an exposed portion of said sidewall while leaving a portion of said thick insulative layer at said bottom of said trench;

forming a thin insulative layer on said exposed portion of said sidewall; and

forming a gate above said portion of said thick insulative layer and adjacent said thin insulative layer in said trench.

20. The method of Claim 19, wherein said forming a thin insulative layer includes thermally oxidizing said sidewall.

21. The method of Claim 20, further comprising:

growing a thin sacrificial oxide layer on said sidewall prior to said forming a thin insulative layer; and

removing said sacrificial oxide layer prior to said forming a thin insulative layer.

22. The method of Claim 19, wherein said forming a gate comprises:

depositing doped polysilicon in said trench; and

etching said doped polysilicon to a level about equal to said surface of said substrate.

23. The method of Claim 19, further comprising growing a thin insulative layer on said sidewall and said bottom prior to said depositing a thick insulative layer.

24. The method of Claim 19, further comprising:

forming a body region in said substrate adjacent said sidewall; and

forming a source region in said body region, said source region adjacent said sidewall and a top surface of said substrate.

25. The method of Claim 19, further comprising forming a high conductivity region in said substrate adjacent to at least said bottom of said trench.

26. A method of fabricating an MIS device, comprising:

providing a semiconductor substrate;

forming a trench in said substrate, said trench including a sidewall and a bottom;

depositing a thick insulative layer on said bottom;

forming a thin insulative layer on said sidewall, said thin insulative layer coupled to said thick insulative layer; and

forming a gate in said trench above said thick insulative layer and adjacent to said thin insulative layer.

27. The method of Claim 26, wherein said depositing a thick insulative layer comprises:

depositing said thick insulative layer on said sidewall and said bottom;

depositing a mask layer in said trench;

etching said mask layer to expose a portion of said thick insulative layer on said sidewall while leaving a portion of said mask layer at said bottom of said trench; and

etching said thick insulative layer to form an exposed portion of said sidewall while leaving a portion of said thick insulative layer at said bottom of said trench.

28. The method of Claim 26, further comprising:

forming a body region in said substrate adjacent said sidewall; and

forming a source region in said body region, said source region adjacent said sidewall and a top surface of said substrate.

29. The method of Claim 26, further comprising forming a high conductivity region in said substrate adjacent to at least said bottom of said trench.

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